MT9519

Current IC, Built-in Magnetic Converter for Sensing Horizontal Magnetic Fields

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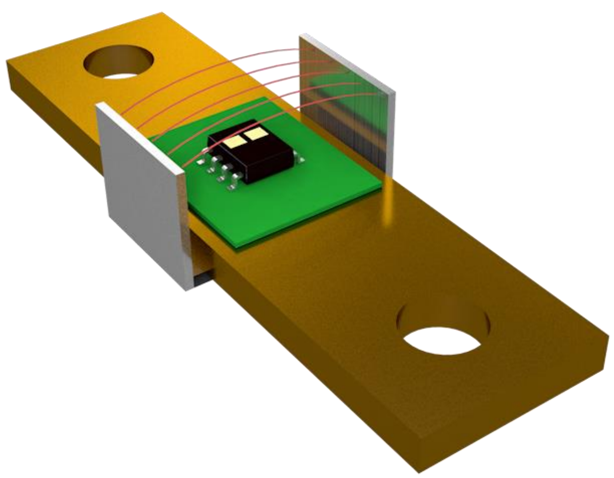
1 Product Description

The MagnTek® MT9519 product series is a current IC that utilizes a built-in magnetic collector to convert a vertical magnetic field into horizontal magnetic dection (HMD). The traditional Horizontal Hall technology is only sensitive to the magnetic flux density applied perpendicular to the IC surface. The sensor IC using HMD technology is only sensitive to the magnetic flux density applied parallel to the surface of the IC. This is achieved by placing two pieces of magnetic conductive metal on the chip. This chip is a highly integrated Hall sensor IC that provides an output signal proportional to the magnetic flux density applied horizontally, making it suitable for current measurement. Due to its small size and use of SOP-8 package, it is very suitable as an open-loop current sensor for PCB or busbar installation. It is suitable for various current ranges from a few amperes to 1000 amperes or higher. MT9519 is user programmable, including current direction, magnetic field sensitivity gain, zero magnetic field signal output, and temperature compensation. It is very suitable for the application of on-board inverters.

The MT9519 series provides customers with SOP-8 package that meets RoHS requirements.



Not to scale

2 Features

- End-of-line programmable
- Typical Accuracy:
  --- ±1.0% (25℃)
- High Linearity:
  --- ±0.5% (25℃)
- High Bandwidth:
  --- 250kHz
- Wide Operating Temperature:
  --- -40℃~150℃
- Fast Output Response Time:
  --- 2.2 μs (typ.)
- Package Option:
  ---SOP-8
- High stability over operation temperature range:
  ---±1.5% (25℃~125℃)
  ---±1.5% (-40℃~25℃)
- Ratiometric Output from Supply Voltage
- Low-Noise Analog Signal Path
- RoHS Compliant: (EU)2015/863

3 Applications

- Vehicle mounted drive motor inverter
- PV string inverters
- Battery management system
- Switching power supplies
- Overcurrent protection

4 Product Overview of MT9519

Part Number	Packing
MT9519CT	SOP-8 Tape & Reel (3000pcs/bag)

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Reversion History

1 Originally Version

5 Functional Block Diagram

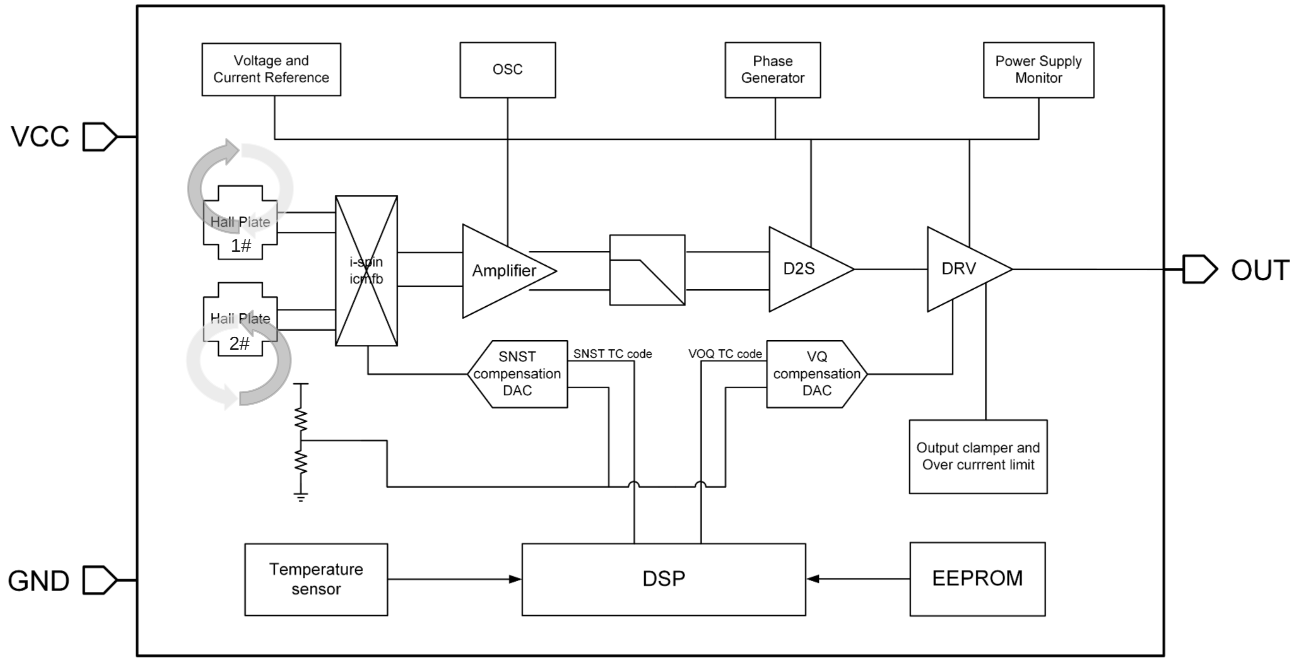

Figure.1 Functional Block Diagram

6 Pin Configuration and Functions

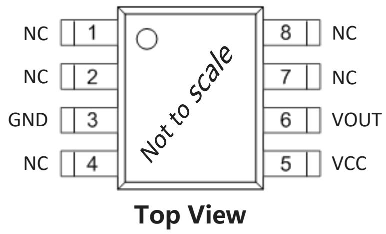

Figure.2 Pin Configuration and Functions (SOP-8)

No.	Name	Description
1, 2	NC	No Internal Connection
3	GND	Signal Ground
4	NC	No Internal Connection
5	VCC	Power Supply
6	VOUT	Analog Output Signal
7, 8	NC	No Internal Connection

7 Naming Specification

Part Number MT9519 (1) CT (2) - 04 (3)

(1) Series Name

(2) Package Type

Type	Package Type
CT	SOP-8

(3) Sensitivity Range

Type	Default Sensitivity
2P5	factory sensitivity：2.5mV/Gs
04	factory sensitivity：4mV/Gs
06	factory sensitivity：6mV/Gs
6P66	factory sensitivity：6.66mV/Gs
10	factory sensitivity：10mV/Gs

8 Selection Guide

Ordering P/N	Output Mode	VCC (V)	Sensitivity (mV/Gs)	Package	Qty per Reel (pcs)
MT9519CT-2P5	Ratio	5	2.5	SOP-8	3000
MT9519CT-04			4		
MT9519CT-06			6		
MT9519CT-6P66			6.66		
MT9519CT-10			10		

9 Typical Application Circuit

The typical application circuits of MT9511series products include a bypass capacitor and a filter capacitor as an additional external components. **CBYPASS capacitor between VCC and GND is necessary.** Magnetic field applied horizontally to chip surface, the analog signal output is measured directly from the VOUT pin

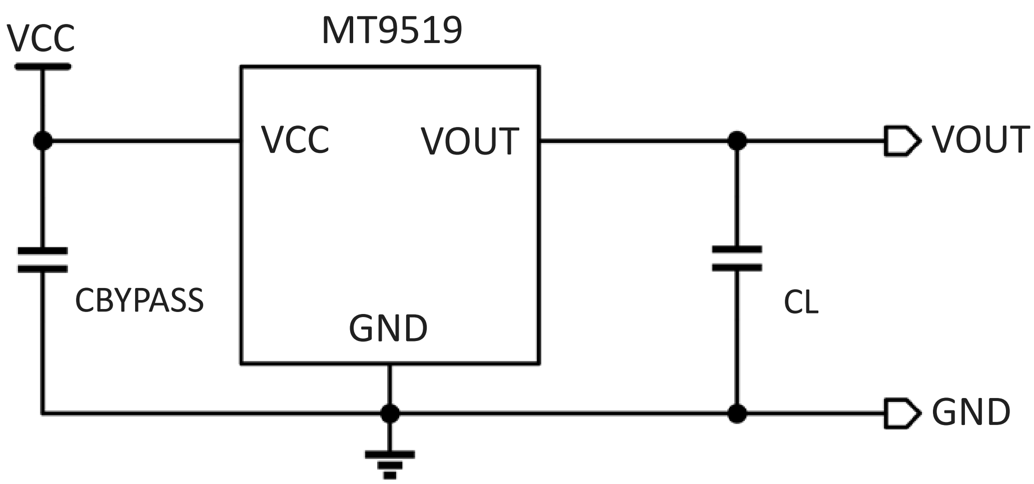

Figure.3 Typical Application Circuit

10 Transfer Characteristics

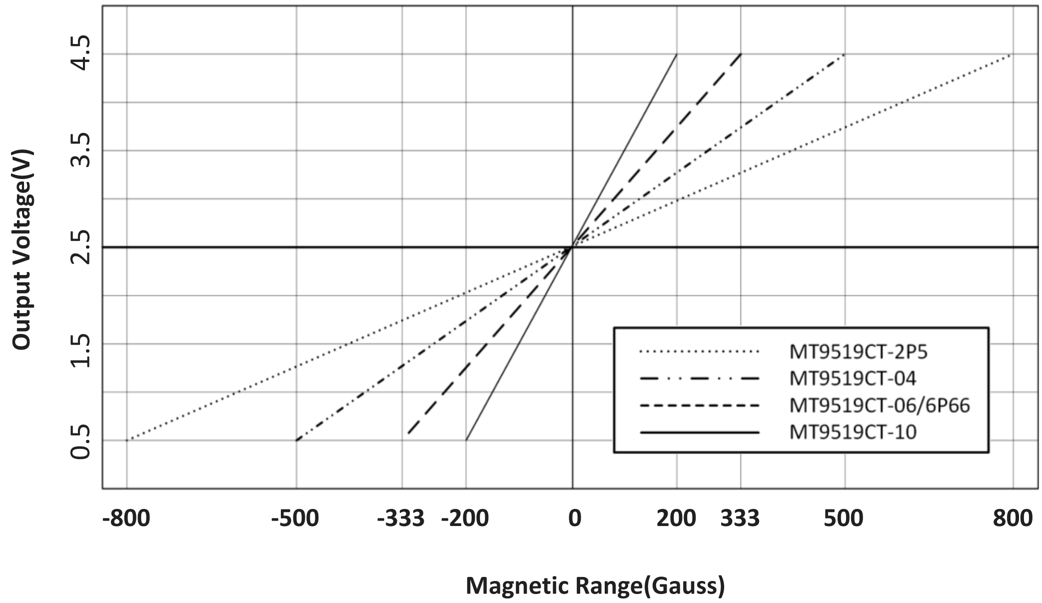

Figure.4 Output Voltage vs. Magnetic Range

The induction direction of the MT9519 series product is shown in the Figure.5.
The current direction flowing through the copper bar is shown as IP.
The magnetic field direction line generated by the magnetic focusing plate is shown as B.

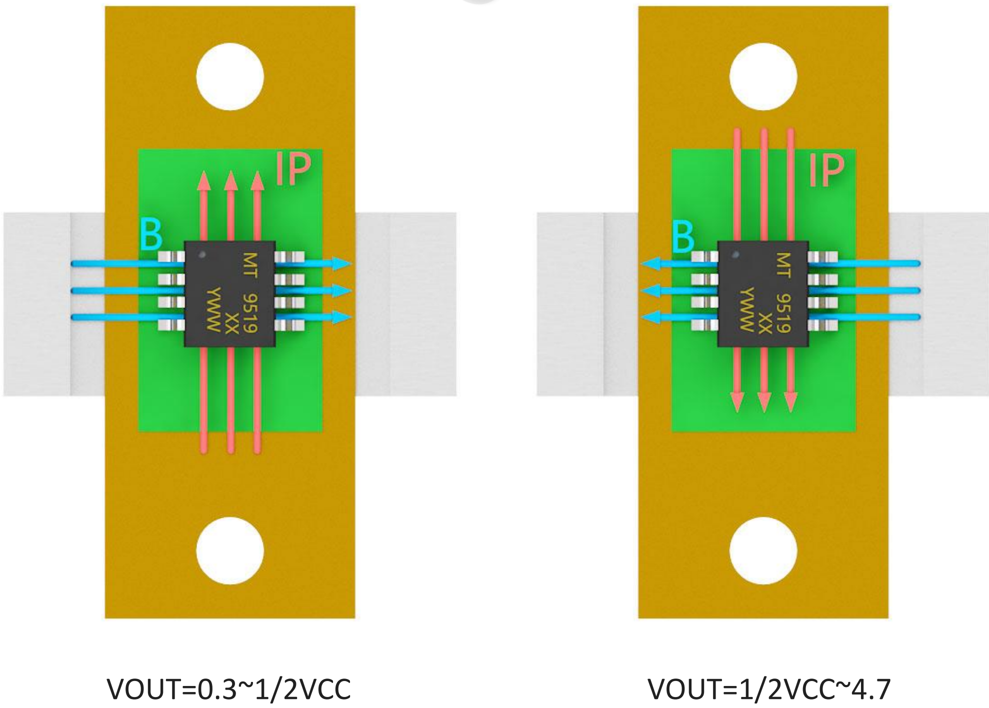

Figure.5 Current Direction & Output Polarity

11 Electrical Magnetic Characteristics

11.1 Absolute Maximum Ratings

Absolute maximum ratings are limited values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

Symbol	Parameters	Min	Max	Units
VCC	Supply Voltage	-	6	V
VRCC	Reverse Battery Voltage	-0.1	-	V
VOUT	Output Voltage	-	VCC+0.5	V
VROUT	Reverse Output Voltage	-0.1	-	V
IOUT(source)	Continuous Output Current(source)	-	55	mA
IOUT(sink)	Continuous Output Current(sink)	-	55	mA
TA	Operating Ambient Temperature	-40	150	℃
TS	Storage Temperature	-50	150	℃
TJ	Junction Temperature	-	165	℃
Endurance	Number of EEPROM Programming Cycles	200	-	cycle

10.2 ESD Ratings

Symbol	Parameters	Reference	Values
VESD	Human-body model(HBM)	AEC-Q100-002	Class IIIA
	Charged-device model(CDM)	AEC-Q100-011	Class C6
	Latch up（Latch up）	AEC-Q100-004	Class IIA

11.3 Electrical Specifications

TA =-40~125 ℃, VCC=5V, CBYPASS=0.1uF (unless otherwise specified)

Symbol	Parameters	Test Condition	Min	Typ	Max	Unit
VCC	Supply Voltage	-	4.5	5	5.5	V
ICC	Supply Current	TA = 25°C	-	15	22	mA
BW	Internal Bandwidth	–3 dB; CL = 1 nF	-	250	-	KHz
TPO	Power on time	TA = 25°C, no CBYPASS, CL = 1nF	-	1.3	-	ms
VUVLOH	Undervoltage Lockout(UVLO) High Voltage	TA = 25°C, VCC rising and device function enabled	-	4	-	V
VUVLOL	Undervoltage Lockout(UVLO) Low Voltage	TA = 25°C, VCC falling and device function disabled	-	3.75	-	V
VUVLOHYS	UVLO Hysteresis	TA = 25°C	-	0.25	-	V
TUVLOD	UVLO Delay Time	TA = 25°C	-	30	-	us
VPORH	Power-On Reset High Voltage	TA = 25°C, VCC rising	-	2.75	-	V
VPORL	Power-On Reset Low Voltage	TA = 25°C, VCC falling	-	2.55	-	V
VPORHYS	Power-On Reset Hysteresis	TA = 25°C	-	0.2	-	V
ISCLP	Source Current of Over-Current-Limit	-	-	55	-	mA
ISCLN	Sink Current of Over-Current-Limit	-	-	55	-	mA
TSCLD	Detect Time for over-Current-Limit	TA = 25°C, IOUT>ISCLP or IOUT<ISCLN	-	10	-	us
TSCLR	Release Time for over-Current-Limit	TA = 25°C	-	1	-	ms
VOL	Analog Output Low Saturation Level	RL>=4.7KΩ	-	-	0.3	V
VOH	Analog Output High Saturation Level	RL>=4.7KΩ	VCC-0.3	-	-	V
CL	Output Cap Load	OUT to GND	-	0.47	1	nF
RL	Output Res Load	Pull-down to GND	4.7	-	-	KΩ
		Pull-up to VCC	4.7	-	-	KΩ
ROUT	DC Output resistance	TA=25°C	-	5	10	Ω
TR	Rise time	B = B(max), TA = 25°C, CL = 1nF	-	2	-	us
TPD	Propagation Delay	B = B(max), TA = 25°C, CL = 1nF	-	1	-	us
TRESP	Response Time	B = B(max), TA = 25°C, CL = 1nF	-	2.2	3	us

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Electrical Specifications(continued)

T_A=-40~125 ℃, V_{CC}=5V, C_{BYPASS}=0.1uF (unless otherwise specified)

Symbol	Parameters	Test Condition	Min	Typ	Max	Unit
VCLP_LO	Clamp Low Output Level	TA = 25℃, RL = 10kΩ to VCC	0.15	-	0.45	V
VCLP_HI	Clamp High Output Level	TA = 25℃, RL = 10kΩ to GND	4.55	-	4.85	V
TCLP	Clamp Low Output Level	TA=25°C	-	8	-	us
IND	Noise Density	Input-referenced noise density; TA = 25°C, SNST=5mV/Gs	-	1	-	mG/√Hz
Accuracy Specification						
ELIN	Nonlinearity Sensitivity Error	TA = 25°C, VCC=5V	-0.5	-	0.5	%
VOQ	Quiescent Voltage Output	TA = 25°C, VCC=5V, B=0Gs	-	0.5*VCC	-	V
VOE	Quiescent Voltage Output Error	TA = 25°C, VCC=5V	-10	-	10	mV
SNST_INIT	Initial Unprogrammed Sensitivity	TA = 25°C, VCC=5V	-	2.5	-	mV/Gs
			-	4	-	mV/Gs
			-	6	-	mV/Gs
			-	6.66	-	mV/GS
			-	10	-	mV/Gs
ERAT_SNST	Ratiometry Sensitivity Error	VCC = 4.5 ~ 5.5 V, TA = 25°C	-1.5	-	1.5	%
ERAT_VOQ	Ratiometry Quiescent Voltage Output Error	VCC = 4.5 ~ 5.5 V, TA = 25°C	-1	-	1	%
ERAT_CLP	Ratiometry Clamp Error	VCC = 4.5 ~ 5.5 V, TA = 25°C	-	±1	-	%
ΔSNST_PKG	Sensitivity Drift Due to Package Hysteresis	TA = 25°C, temperature cycling: from 25°C to 150°C and back to 25°C	-	±1.25	-	%
Programming Specification						
VOQ_STEP	Average Quiescent Voltage Output Programming Step Size	TA = 25°C, VCC=5V	-	±1.25	-	mV
EVOQ_STEP	Quiescent Voltage Output Programming Resolution	TA = 25°C, VCC=5V	-	±0.625	-	mV
SNST_PR	Sensitivity Programmed Range	TA = 25°C, VCC=5V	2	-	20	mV/Gs
SNST_STEP	Average Sensitivity Programming Step Size	TA = 25°C, VCC=5V	-	±0.3125	-	%
ESNST_STEP	Sensitivity Programming Resolution	TA = 25°C, VCC=5V	-	±0.1562	-	%

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Electrical Specifications(continued)

T_A=-40~125 ℃, V_{CC}=5V, C_{BYPASS}=0.1uF (unless otherwise specified)

Symbol	Parameters	Test Condition	Min	Typ	Max	Unit
Factory Temperature Coefficient Programed Specification						
ΔSNST_TC	Sensitivity Drift Through Temperature Range	TA = 25°C to 125°C	-1.5	-	1.5	%
		TA = –40°C to 25°C	-1.5	-	1.5	%
SNST_TC_STEP	Average Sensitivity Temperature Compensation Step Size		-	±0.07	-	%/℃
ΔVOE_TC	Quiescent Voltage Output Drift Through Temperature Range	TA = 25°C to 125°C	-10	-	10	mV
		TA = –40°C to 25°C	-10	-	10	mV
VOQ_TC_STEP	Average Quiescent Voltage Output Temperature Compensation Step Size		-	1.25	-	mV/℃
Lock Bit Programming						
EELOCK_BIT	EEPROM Lock Bit		-	1	-	bit

12 Characteristic Definitions

Power On Time---TPO

When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before responding to an input magnetic field.
The Power-On Time (TPO) is defined as the time taken between the supply reaching the minimum operating voltage VCCmin (t1), and the output voltage to settling to within ±10% of its steady state value under an applied magnetic field (t2) (See Figure 6).

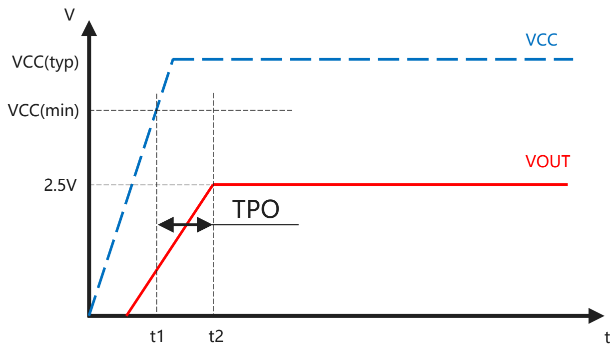


Figure.6 **Power On Time Definition**

Propagation Delay---TPD

The time interval between a) when the primary current signal reaches 20% of its final value, and b) when the output reaches 20% of its final value (see Figure.7).

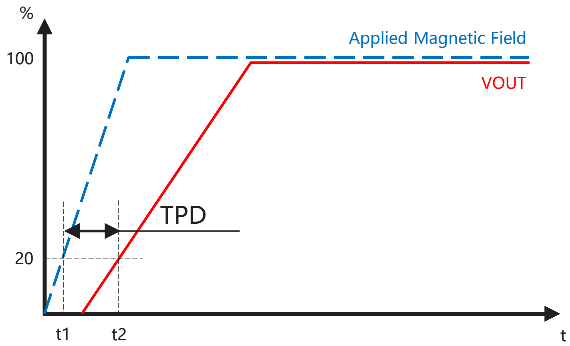


Figure.7 **Propagation Delay Definition**

Rise Time---TR

Rise Time is the time interval between the sensor VOUT reaching 10% of its full scale value (t1), and it reaching 90% of its full scale value (t2). (see Figure.8). Both TR and TRESP can be negatively affected by any eddy current losses created if a conductive ground plane is used.

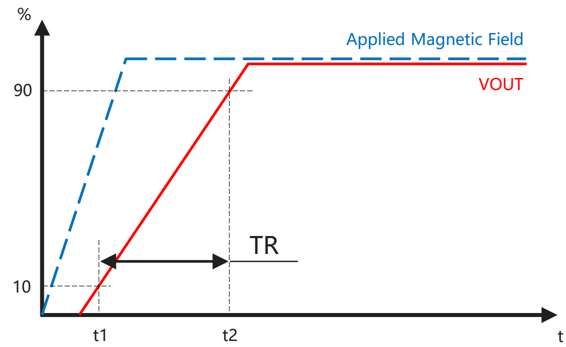


Figure.8 **Rise Time Definition**

Response Time---TRESP

The time interval between a) when the primary current signal reaches 80% of its final value, and b) when the sensor reaches 80% of its output corresponding to the applied current. (see Figure.9). Both TR and TRESP can be negatively affected by any eddy current losses created if a conductive ground plane is used.

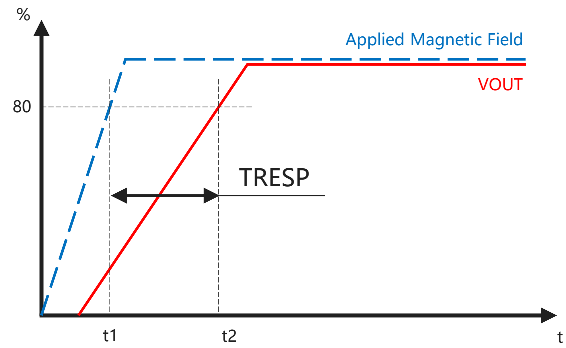


Figure.9 **Response Time Definition**

Delay to Clamp---TCLP

A large magnetic input step may cause the clamp to overshoot its steady state value. The Delay to Clamp (TCLP) is defined as the time it takes for the output voltage to settle within ±1% of its steady state value, after initially passing through its steady state voltage (see Figure.10)。

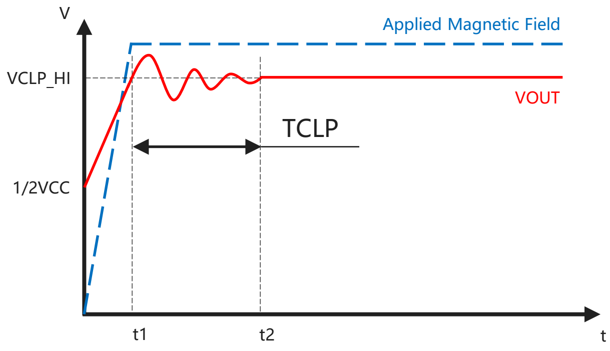


Figure.10 **Propagation Delay Definition**

Quiescent Voltage Output---VOQ

In the quiescent state (no significant magnetic field: B = 0GS), the output (VOQ), has a constant ratio to the supply voltage (VCC), throughout the entire operating ranges of VCC and ambient temperature (TA)，VOQ=0.5*VCC。

Quiescent Voltage Output Drift Through Temperature Range---ΔVOQ_TC

Due to internal component tolerances and thermal considerations, the Quiescent Voltage Output (VOQ), may drift from its nominal value through the operating ambient temperature (TA). The Quiescent Voltage Output Drift Through Temperature Range, Δ VOQ_TC, is defined as:

$$\Delta VOQ\_TC = VOQ(TA) - VOQ\_EXPECT(TA)$$

VOQ_TC should be calculated using the actual measured values of VOQ(TA) and VOQ_EXPECT(TA) rather than programming target values

Sensitivity---SNST

The magnetic field horizontal to the packaging marking surface is linearly related to the output voltage. The larger the magnetic field, the greater the change in output voltage, and vice versa, the smaller the change in output voltage. This ratio is specified as the magnetic sensitivity SNST (mv / Gs) of the chip, is defined as:

$$SNST = \frac{V_{OUT(BPOS)} - V_{OUT(BNEG)}}{BPOS - BNEG}$$

where BPOS and BNEG are two magnetic fields with opposite polarities.

Sensitivity Drift Through Temperature Range---ΔSNST_TC

The temperature coefficient effect of sensitivity can cause magnetic sensitivity to deviate from its expected value in the operating ambient temperature range (TA). The Sensitivity Drift Through Temperature Range, Δ SNST_TC, is defined as:

$$\Delta SNST\_TC = \frac{SNST(TA) - SNST\_EXPECT(TA)}{SNST\_EXPECT(TA)} * 100\%$$

Sensitivity Drift Due to Package Hysteresis---ΔSNST_PKG

The stress effect during packaging can cause magnetic sensitivity to deviate from its expected value. The Sensitivity Drift Through Temperature Range, ΔSNST_PKG, is defined as:

$$\Delta SNST\_PKG = \frac{SNST\_25℃\_2 - SNST\_25℃\_1}{SNST\_25℃\_1} * 100\%$$

where SNST_25 ℃_1 is programmed value of sensitivity at TA=25℃, and SNST_25℃_2 is the value of sensitivity at TA=25℃, after temperature cycling from TA to 150℃/168 hours and back to 25℃

Nonlinearity Sensitivity Error---ELIN

Ideally input magnetic field vs sensor output function is a straight line. The non-linearity is an indication of the worst deviation from this straight line. The ELIN in % is defined as:

$$ELIN = \left(\frac{SNST\_B1}{SNST\_B2} - 1\right) * 100\%$$

Where:

$$SNST\_B1 = \left(\frac{VOUT\_BPOS1 - VOUT\_BNEG1}{BPOS1 - BNEG1}\right)$$

$$SNST\_B2 = \left(\frac{VOUT\_BPOS2 - VOUT\_BNEG2}{BPOS2 - BNEG2}\right)$$

and BPOSx and BNEGx are positive and negative magnetic fields, with respect to the quiescent voltage output such that |BPOS2| = |BNEG2| = Bmax, and |BPOS2| = 2 * |BPOS1| and |BNEG2| = 2 * |BNEG1|.

Symmetry Sensitivity Error---ESYM

The magnetic sensitivity of MT9519 device is constant for any applied magnetic fields of equal magnitude and opposite polarities.
Symmetry Error (ESYM) is measured and defined as:

$$ESYM=\left(\frac{SNST\_BPOSx}{SNST\_BNEGx}-1\right)*100\%$$

Where:

$$SNST\_BPOSx=\frac{VOUT\_Bx-VOQ}{Bx}$$

$$SNST\_BNEGx=\frac{VOQ-VOUT\_Bx}{Bx}$$

BPOSx and BNGx are positive and negative magnetic fields such that |BPOSx| = |BNEGx|.

Ratiometry Error---ERAT

The MT9519 device features ratiometric output. This means that the Quiescent Voltage Output (VOQ), magnetic sensitivity (SNST) and Output Voltage Clamp (VCLP_HI, VCLP_LO), are proportional to the Supply Voltage (VCC). In other words, when the VCC increases or decreases by a certain percentage, each characteristic also increases or decreases by the same percentage. Error is the difference between the measured change in the VCC relative to 5V, and the measured change in each Characteristic

Ratiometry Quiescent Voltage Output Error---ERAT_VOQ

ERAT_VOQ, for a given supply voltage, is defined as:

$$ERAT\_VOQ=\left(\frac{VOQ(VCC)/VCC}{VOQ(5V)/5V}-1\right)*100\%$$

Ratiometry Sensitivity Error--ERAT_SNST

ERAT_SNST, for a given supply voltage, is defined as:

$$ERAT\_SNST=\left(\frac{SNST\_B1(VCC)/VCC}{SNST\_B1(5V)/5V}-1\right)*100\%$$

Ratiometry Clamp Error---ERAT_CLP

ERAT_CLP, for a given supply voltage, is defined as:

$$ERAT\_CLP=\left(\frac{VCLP(VCC)/VCC}{VCLP(5V)/5V}-1\right)*100\%$$

Where VCLP is either VCLP_HI or VCLP_LO.

Over Current Limit---ISCLP & ISCLN

The MT9519 has over-current protection function. When IOUT≥ISCLP or ISCLN, the output driver will be closed and the output will be turned into high resistance state.

Power-On Reset---POR, Undervoltage Lockout---UVL

The descriptions in this section assume temperature = 25°C, no output load (RL, CL) , and no significant magnetic field is present.

Power-Up. At power-up, as VCC ramps up, the output is in the following power supply voltage state. When VCC exceeds VPORH, the chip will enters the handshake protocol state. When VCC exceeds VUVLOH, the output will go to 1/2*VCC or 2.5V, at this time, the chip is in normal working state.

Power-Down. If VCC drops below VUVLOL, the output will be in a high-impedance state. If VCC drops below VPORL, the output is in the following power supply voltage state (See Figure. 11).

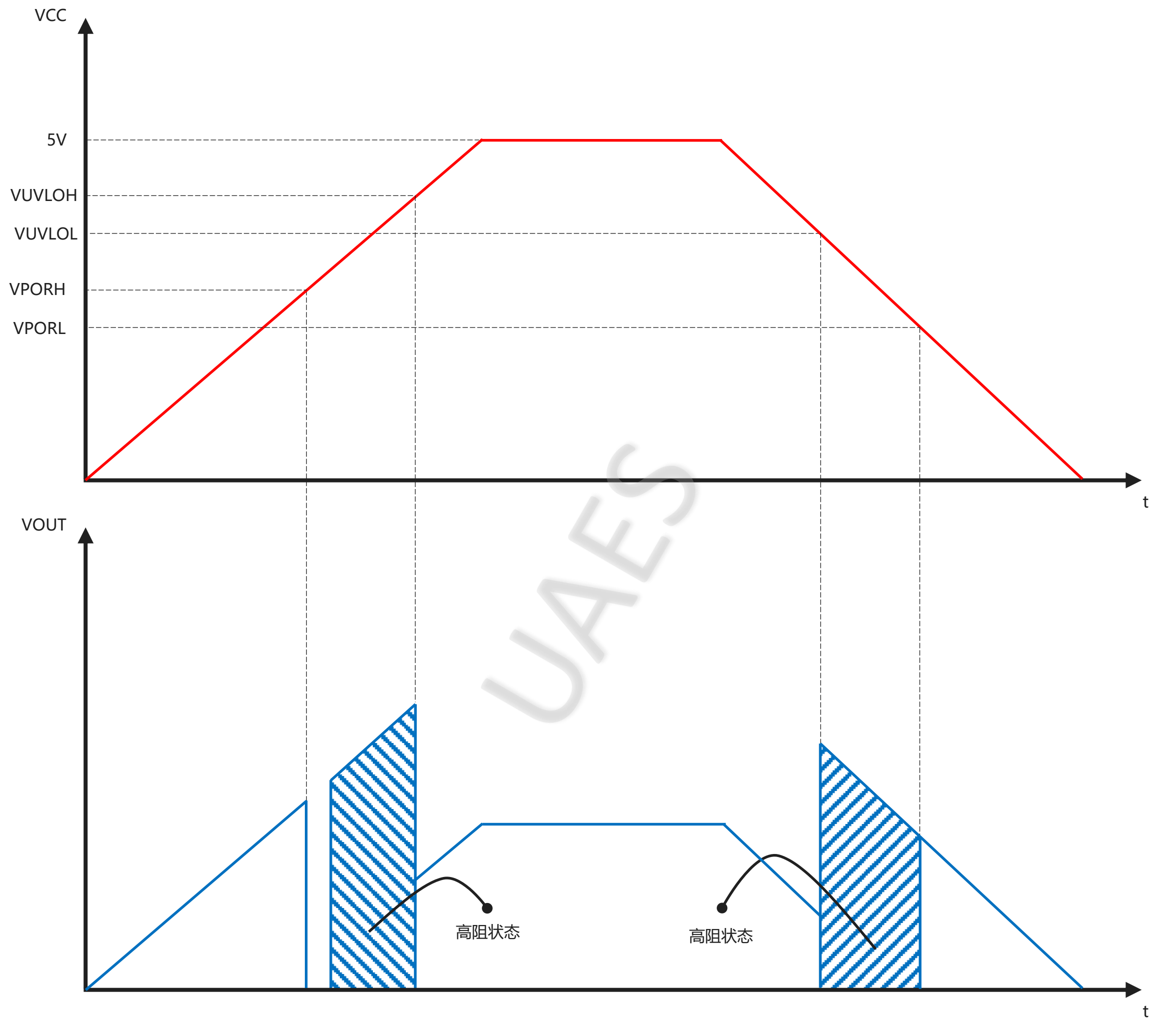
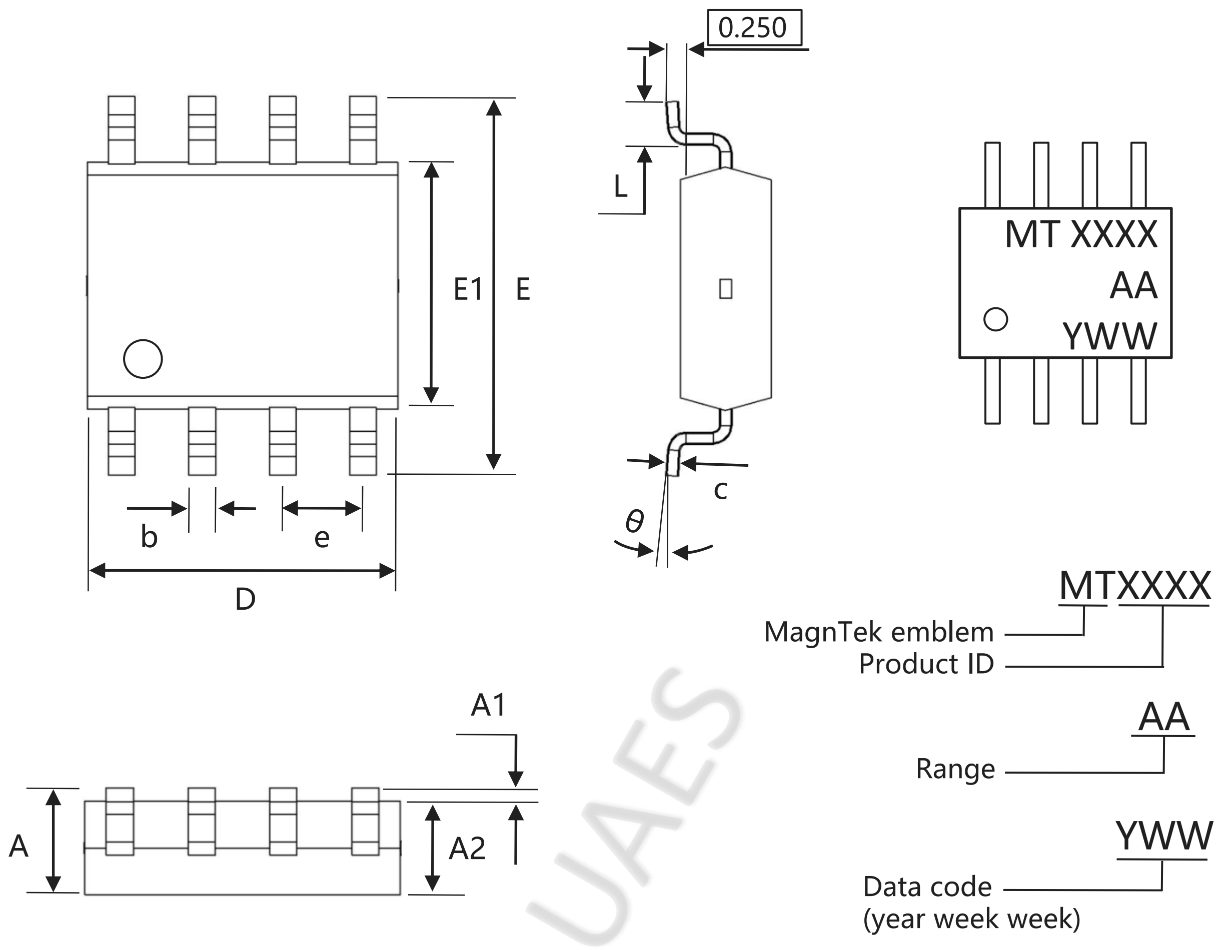


Figure.11 **POR and UVL Definition**

13 Package Material Information (For Reference Only – Not for Tooling Use)

13.1 SOP-8 Package Information



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	1.450	1.750	0.057	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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